REMARKS

The following remarks are provided in response to the Final Office Action mailed April 5, 2007, in which the Examiner:

- allowed claims 35-40, 42-48 and 50-62.
- rejected claims 63-70 under 35 U.S.C. §103(a) as being unpatentable over U.S. 2003/0132466 to Shin et al. (hereinafter Shin) in view of JP 05226361 to Matshuhashi (hereinafter Matsuhashi), WO 00/77828 to Stolk et al. (hereinafter Stolk) and U.S. 6,737,309 to Matsuo (hereinafter Matsuo).

The applicants respectfully request reconsideration of the above referenced patent application for the following reasons:

Allowable Subject Matter

The Examiner allowed claims 35-40, 42-48 and 50-62. The Applicants respectfully acknowledge the Examiner's allowance of this subject matter.

Claims 63-70 rejection under 35 U.S.C. §103(a)

Claims 63-70 are rejected under 35 U.S.C. §103(a) as being unpatentable over Shin in view of Matsuhashi, Stolk and Matsuo. The Examiner notes that independent claim 63 does not specifically require that the central portion of the gate electrode actually contact the gate dielectric layer (*see* Examiner's remarks, p. 2, 2nd paragraph, Office Action dated May 5, 2007). The Applicants accordingly herein amend independent claim 63, from which claims 64-70 depend, and respectfully request that the

Examiner reconsider claims 63-70 in view of the amendments and the following arguments.

In claims 63-70, the Applicants teach and claim a transistor comprising a dielectric layer above a substrate and a trench in the dielectric layer, wherein the bottom of the trench is directly above the substrate. A gate dielectric layer is on the bottom of the trench. A gate electrode is in the trench and is comprised of a central portion and a pair of outer portions, wherein the outer portions are each comprised of a sidewall region and an extension region. The central portion is directly adjacent to the sidewall region and directly above the extension region of each of the outer portions. The bottom surfaces of the central portion and the pair of outer portions of the gate electrode are directly on the gate dielectric layer on the bottom of the trench. The workfunction of the pair of outer portions is different than the workfunction of the central portion. Finally, a pair of source/drain regions is in the substrate on opposite sides of the pair of outer portions of the gate electrode. That is, the applicants teach and claim a transistor having **a gate electrode comprising a pair of outer portions and a central portion, wherein each outer portion comprises a sidewall region and an extension region, and wherein the central portion is directly on the gate dielectric layer** (outer portion with sidewall region and extension region: *see* item "222" of Fig. 2, item "322" of Figs. 3G-3K, and paragraphs [0011] and [0026]).

None of Shin, Matshuhashi nor Stolk disclose a transistor having a gate electrode comprising a pair of outer portions and a central portion, wherein each outer portion comprises a sidewall region and an extension region, and wherein the central portion is

directly on the gate dielectric layer, as taught and claimed by the Applicants. All three references do disclose a transistor having three portions of a gate electrode. However, the outer regions of the gate electrodes of Shin, Matshuhashi and Stolk are fabricated by an anisotropic etch process and therefore only comprise sidewall regions. The Applicants teach fabricating outer regions of a gate electrode by angled deposition, thus forming both sidewall and extension regions for each outer portion of the gate electrode. Thus, **Shin, Matshuhashi and Stolk disclose a gate electrode having outer portions comprised of only a sidewall region**, whereas **the Applicants teach a gate electrode having outer portions comprised of both a sidewall region and an extension region**.

The Examiner relies on Matsuo to disclose a transistor having a central gate portion overlying extension portions of an outer gate. However, Matsuo fails to disclose a transistor wherein the central portion of a gate electrode is directly on the gate dielectric layer. The extension regions of the two outer gates of Matsuo are connected. Therefore, the central gate electrode of Matsuo is not on the gate dielectric layer, as taught and claimed by the Applicants. Thus, none of Shin, Matsuhashi, Stolk nor Matsuo, alone or in combination, disclose a transistor having a gate electrode comprising a pair of outer portions and a central portion, wherein each outer portion comprises a sidewall region and an extension region, and wherein the central portion is directly on the gate dielectric layer, as taught and claimed by the Applicants.

CONCLUSION

The Applicants submit that they have overcome the Examiner's rejections of the claims and that they have the right to claim the invention as set forth in the listed claims. The Examiner is respectfully requested to contact the undersigned by telephone if it is believed that such contact would further the examination of the present application.

Pursuant to 37 C.F.R. 1.136(a)(3), applicant(s) hereby request and authorize the U.S. Patent and Trademark Office to (1) treat any concurrent or future reply that requires a petition for extension of time as incorporating a petition for extension of time for the appropriate length of time and (2) charge all required fees, including extension of time fees and fees under 37 C.F.R. 1.16 and 1.17, to Deposit Account No. 02-2666.

Respectfully submitted,

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